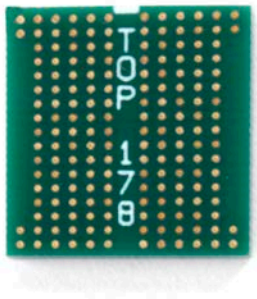
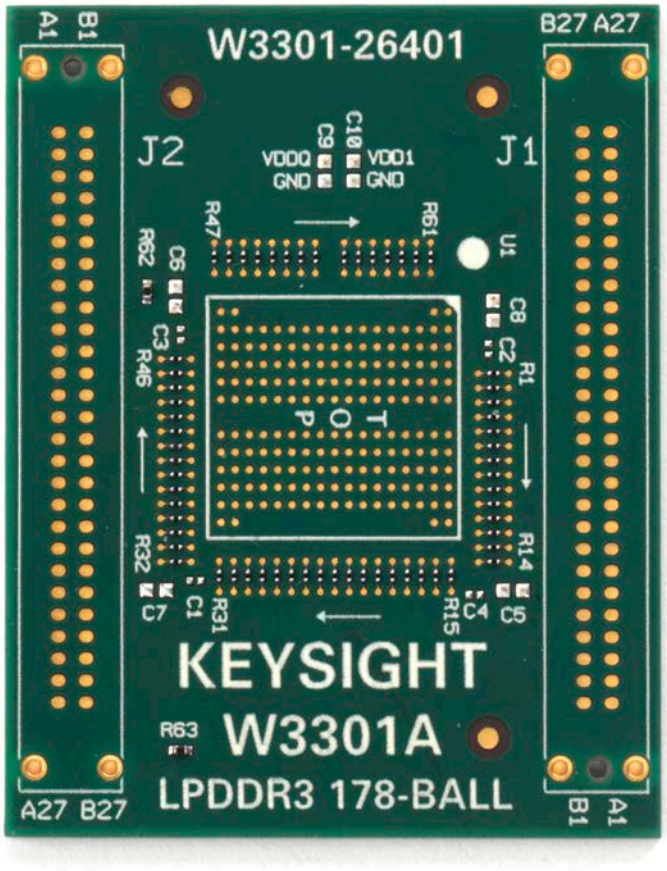
Keysight W3301A
LPDDR3 178-ball Rigid BGA Interposer

Data Sheet





KEYSIGHT TECHNOLOGIES

Unlocking Measurement Insights

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Introduction

The Keysight Technologies, Inc. W3301A LPDDR3 BGA interposer enables probing of embedded memory LPDDR3 178-ball DRAM from the ball grid array with Keysight U4164A logic analyzers.

The W3301A LPDDR3 178-ball rigid BGA interposer is designed to capture data rates in excess of 1866 Mb/s.

The LPDDR3 BGA interposer advantage

Features	Benefits
Direct connection to the LPDDR3 BGA balls using a riser	Eliminates reflections from mid-bus probing methods. Also eliminates design time, prototype builds and trace routing required to design in alternative probing methods
Supports LPDDR3 178-ball DRAM at data rates exceeding 1866 Mb/s	
Probes a 178-ball LPDDR3 single channel x32 DRAM with JEDEC MO-311C footprint variations xA and xB with a package size of 11.5 x 11 mm to 13.5 x 13 mm	
For tight keep-out volume applications, a separate LPDDR3 178-ball riser is included	
LPDDR3, decode, functional compliance and performance analysis using optional software tools	Accelerates navigation and insight of information captured in the logic analyzer trace via multiple different graphs and views of condensed analysis of LPDDR3 traces
Compatible with APS (advanced probe settings) to enable DQ (data) capture over 1866 Mb/s	Provides larger eyes to logic analyzer for accurate signal capture via internal logic analyzer comparator compensation
Leaded or lead-free solder supported	Works easily with all solder finishes. Designed to tolerate lead-free soldering temperature profiles
Contract manufactures available for those without the in-house expertise or facilities for soldering BGAs	Eliminates the need to develop BGA soldering expertise
Measurement timing skew within ± 25 ps achieved by matched trace lengths from DRAM balls to Soft Touch Pro pads for logic analyzer connection	Accuracy for timing measurements
Unpopulated capacitor pads on the interposer are available for optional power supply decoupling capacitors or voltage probe points	Allows flexibility in testing for individual systems under test

W3301A LPDDR3 BGA Interposer

Memory family	DRAM package	Interposer construction	Data rates	Signal coverage	Connections	Use model
LPDDR3	– 178-ball – 0.8 mm x 0.65 mm pitch – JEDEC MO-311 footprint variation MO-311 with maximum DRAM package size of 13.5 x 13 mm fit on top of W3301A without an additional (optional) riser or socket to provide clearance for the tipR components	Rigid	In excess of 1866 Mb/s	Command address – All CA Control RESET – CKE0, CKE1, ODT, CS0, CS1, CK_A Data – All DQ – All DQSt	Connects using qty (2) E5406A Soft Touch Pro probes and qty (4) U4201A logic analyzer cables	Debug and functional validation for LPDDR3 178-ball DRAM configured as single channel system

W3301A LPDDR3 178-ball Rigid BGA Interposer

The W3301A LPDDR3 178-ball BGA interposer is designed to satisfy functional debug and validation for LPDDR3 178-ball chip down systems.

The W3301A probes signals from the LPDDR3 178-ball DRAM footprint and routes the probed signals to two Soft Touch Pro connector footprints. Connection to the Keysight logic analyzer is through two E5406A Soft Touch Pro probes and four U4201A cables into a single U4164A logic analyzer.

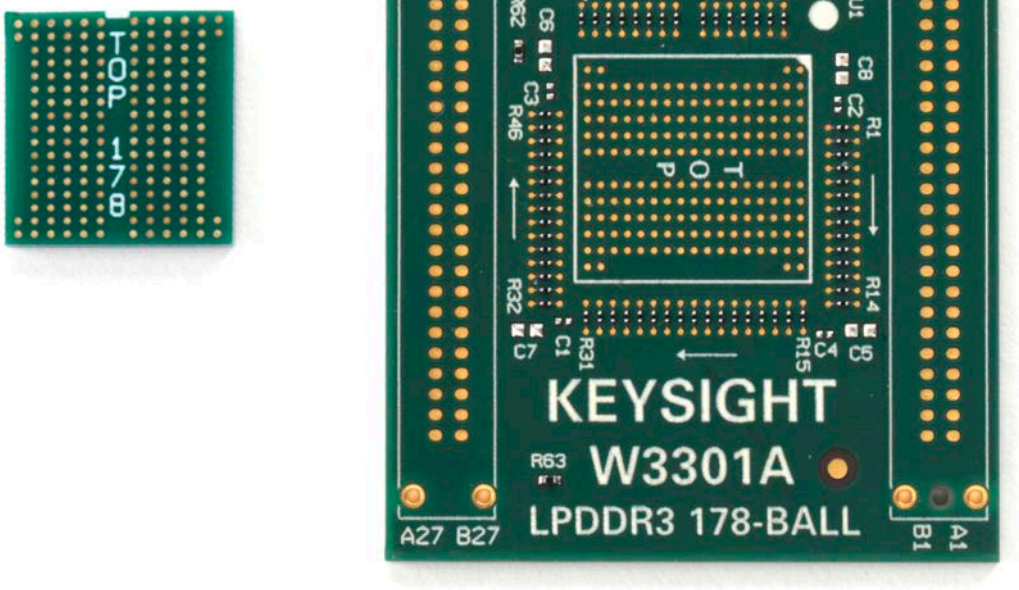


Figure 1. Top view of W3301A LPDDR3 178-ball rigid BGA interposer and riser.

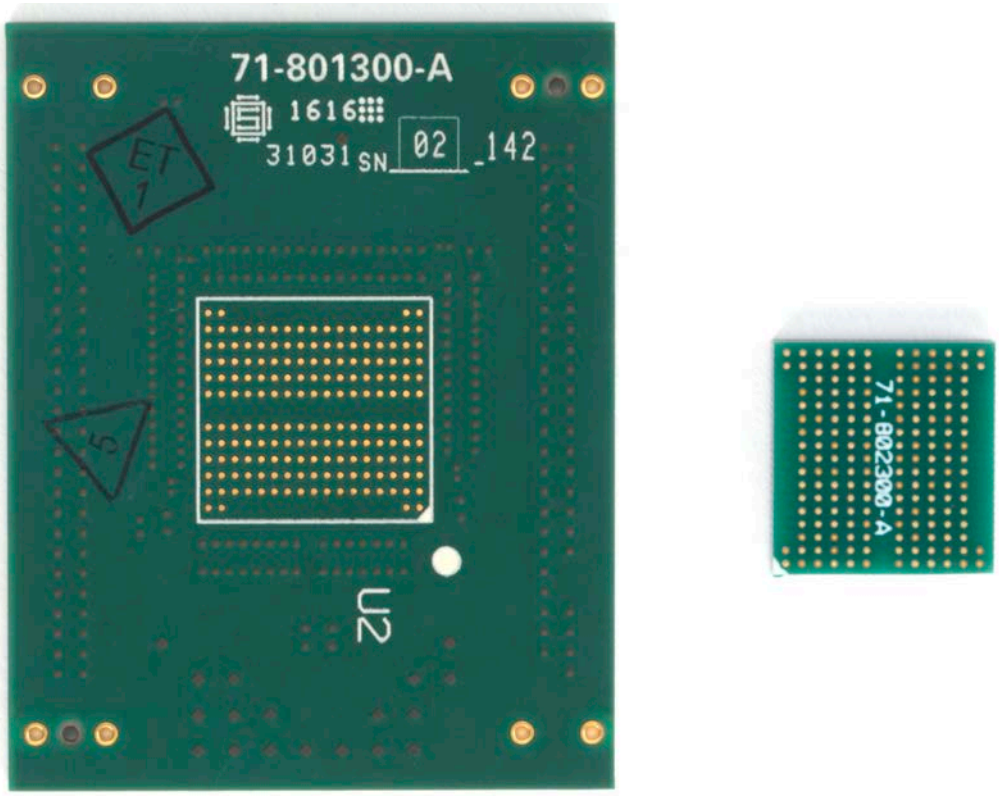


Figure 2. Bottom view of W3301A LPDDR3 178-ball rigid BGA interposer and riser.

Technical characteristics

●	1	2	3	4	5	6	7	8	9	10	11	12	13
A	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU
B	DNU	GND	ZQ0	ZQ1	GND	GND		DQ31	DQ30	DQ29	DQ28	GND	DNU
C		CA9	GND	NC	GND	GND		DQ27	DQ26	DQ25	DQ24	VDDQ	
D		CA8	GND	VDD2	VDD2	VDD2		DM3	DQ15	DQS3_t	DQS3_c	GND	
E		CA7	CA6	GND	GND	GND		VDDQ	DQ14	DQ13	DQ12	VDDQ	
F		VDDCA	CA5	GND	GND	GND		DQ11	DQ10	DQ9	DQ8	GND	
G		VDDCA	GND	GND	VDD2	GND		DM1	GND	DQS1_t	DQS1_c	VDDQ	
H		GND	VDDCA	VrefCA	VDD2	VDD2		VDDQ	VDDQ	GND	VDDQ	VDD2	
J		CK_c	CK_t	GND	VDD2	VDD2		ODT	VDDQ	VDDQ	VrefDQ	GND	
K		GND	CKE0	CKE1	VDD2	VDD2		VDDQ	NC	GND	VDDQ	VDD2	
L		VDDCA	CS0_n	CS1_n	VDD2	GND		DM0	GND	DQS0_t	DQS0_c	VDDQ	
M		VDDCA	CA4	GND	GND	GND		DQ4	DQ5	DQ6	DQ7	GND	
N		CA2	CA3	GND	GND	GND		VDDQ	DQ1	DQ2	DQ3	VDDQ	
P		CA1	GND	VDD2	VDD2	VDD2		DM2	DQ0	DQS2_t	DQS2_c	GND	
R		CA0	NC	GND	GND	GND		DQ20	DQ21	DQ22	DQ23	VDDQ	
T	DNU	GND	GND	GND	GND	GND		DQ16	DQ17	DQ18	DQ19	GND	DNU
U	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU

Figure 3. Signals routed from W3301A into logic analyzer.
- DQ and DQS highlighted in 'green' are probed.
- CK and CKE highlighted in 'yellow' are probed.
- CA and ODT highlighted in 'red' are probed.

Signal access

All signals, including power and ground signals, are passed between the circuit board and LPDDR3 DRAM through vias in the W3301A LPDDR3 178-ball BGA interposer.

LPDDR3 signal group logic analyzer signal access

Command/address
- All channel CA

Control and other signals
- All

Data
- All except DQS0_c_A, DQS1_c_A

Power
- LPDDR3 device power is not monitored by the logic analyzer
- Passed through the interposer through vias

W3301A interposers include separate ground, 1.1 V (VDD2/VDDQ) and 1.8 V (VDD1) planes. For additional installation information, refer to the W3301A installation guide at **http://literature.cdn.keysight.com/litweb/pdf/W3301-97000.pdf**.

Dimensional drawings

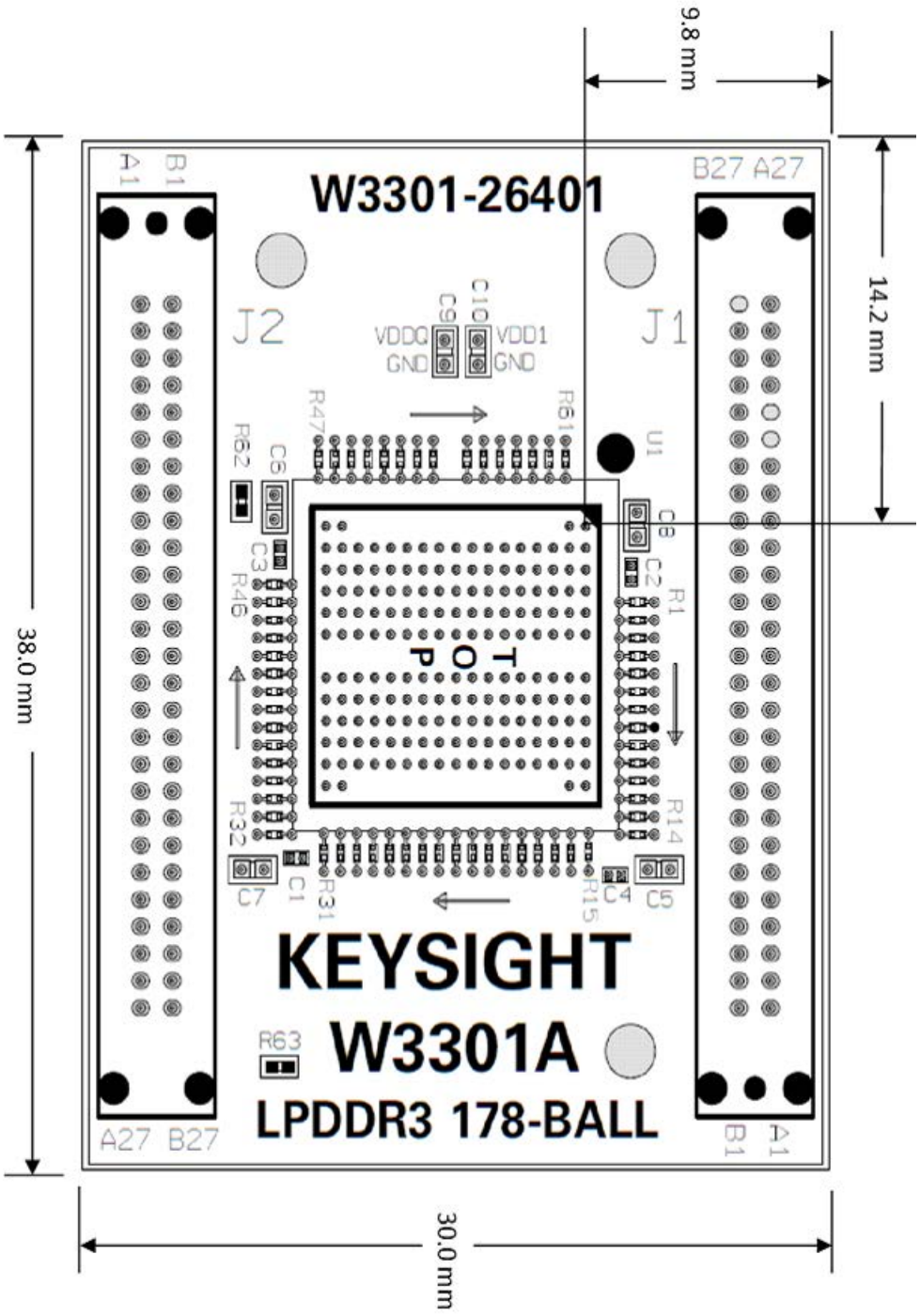
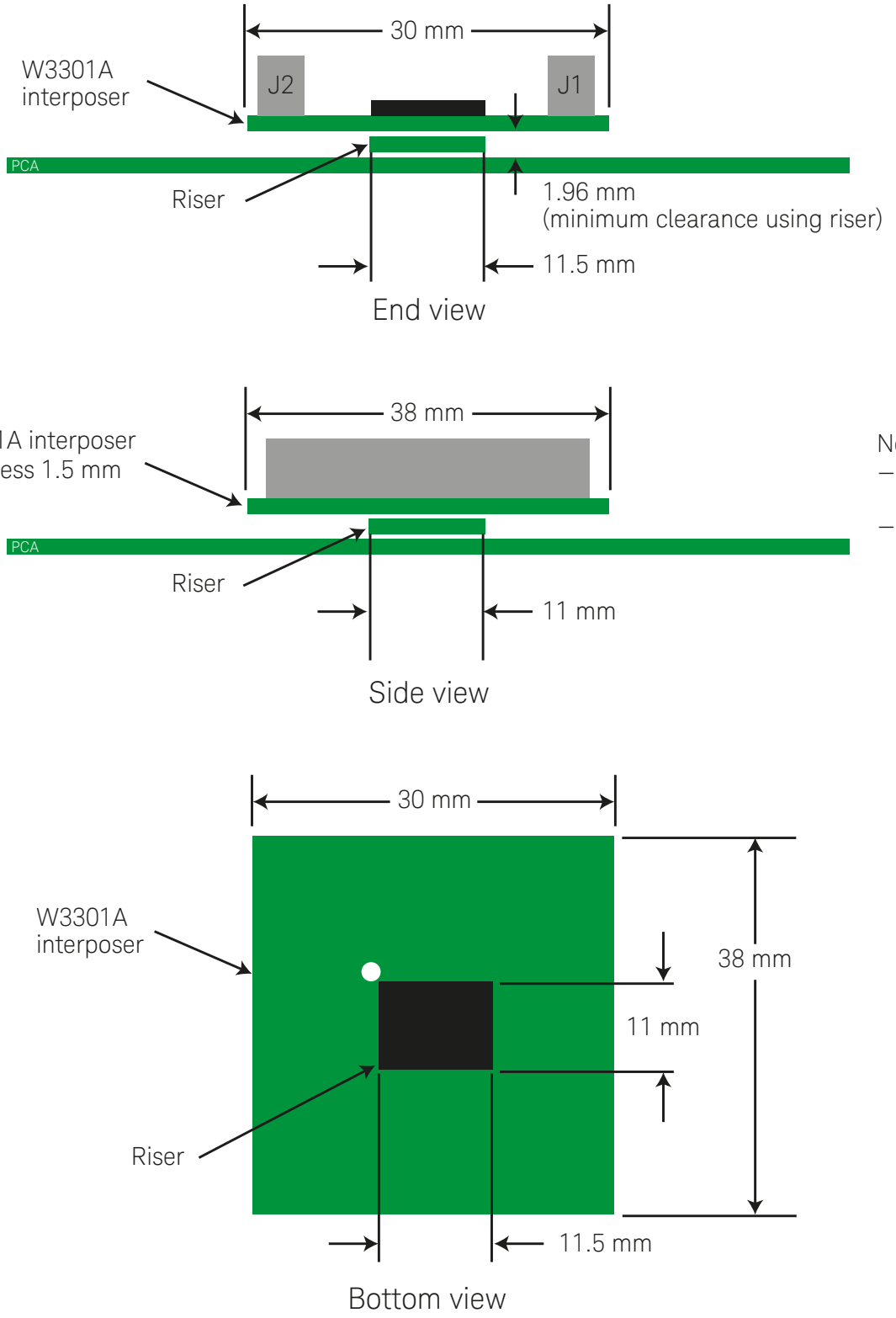


Figure 4. Top dimensional view of W3301A. (W3301A thickness is 1.5 mm ± 10%.)

Note: W3301A includes pads for optional VDDQ (C9) and VDD1 (C10) bypass capacitors on the top of the W3301A. The VDDQ and VDD1 capacitor pads provide easy access for monitoring VDDQ and VDD1 with a Keysight N7020A power rail probe for use with the MSOS804A Infiniium S-Series oscilloscope. The oscilloscope trace of the power rail noise can be easily imported into the Keysight logic analyzer waveform for correlation of power noise to traffic flow using ViewScope. ViewScope is provided at no extra charge in the standard logic analyzer application software.



Note:
- All dimensions are nominal
- There are no components on the bottom of the W3301A interposer

Figure 5. End, side and bottom dimensional views of W3301A KOV (keep out volume) with riser.

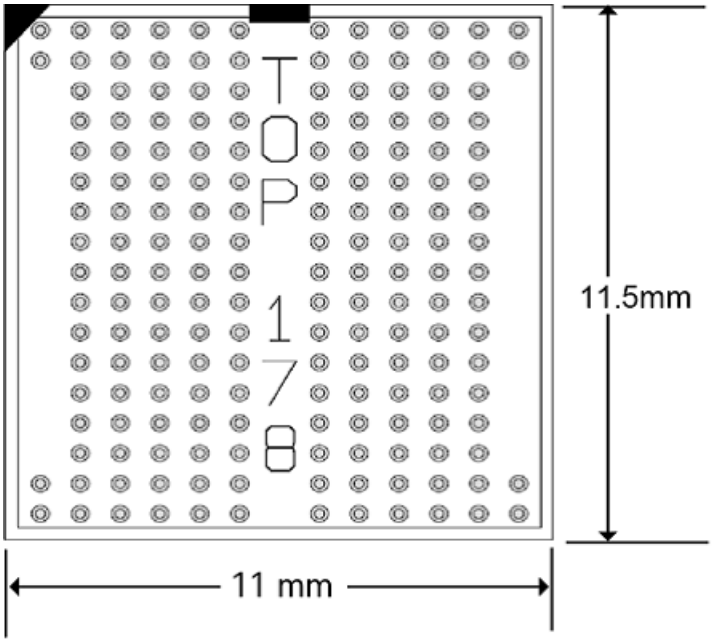


Figure 6. LPDDR3 178-ball riser. (LPDDR3 riser is 2.16 mm thick ± 10%.)

Connecting the W3301A with E5406A Soft Touch Pro probes and U4201A cables to a U4164A logic analyzer

In a W3301A interposer setup, you connect the E5406A Soft Touch Pro probes and U4201A cables to U4164A logic analyzer pods per the mapping shown in the Figure 7.

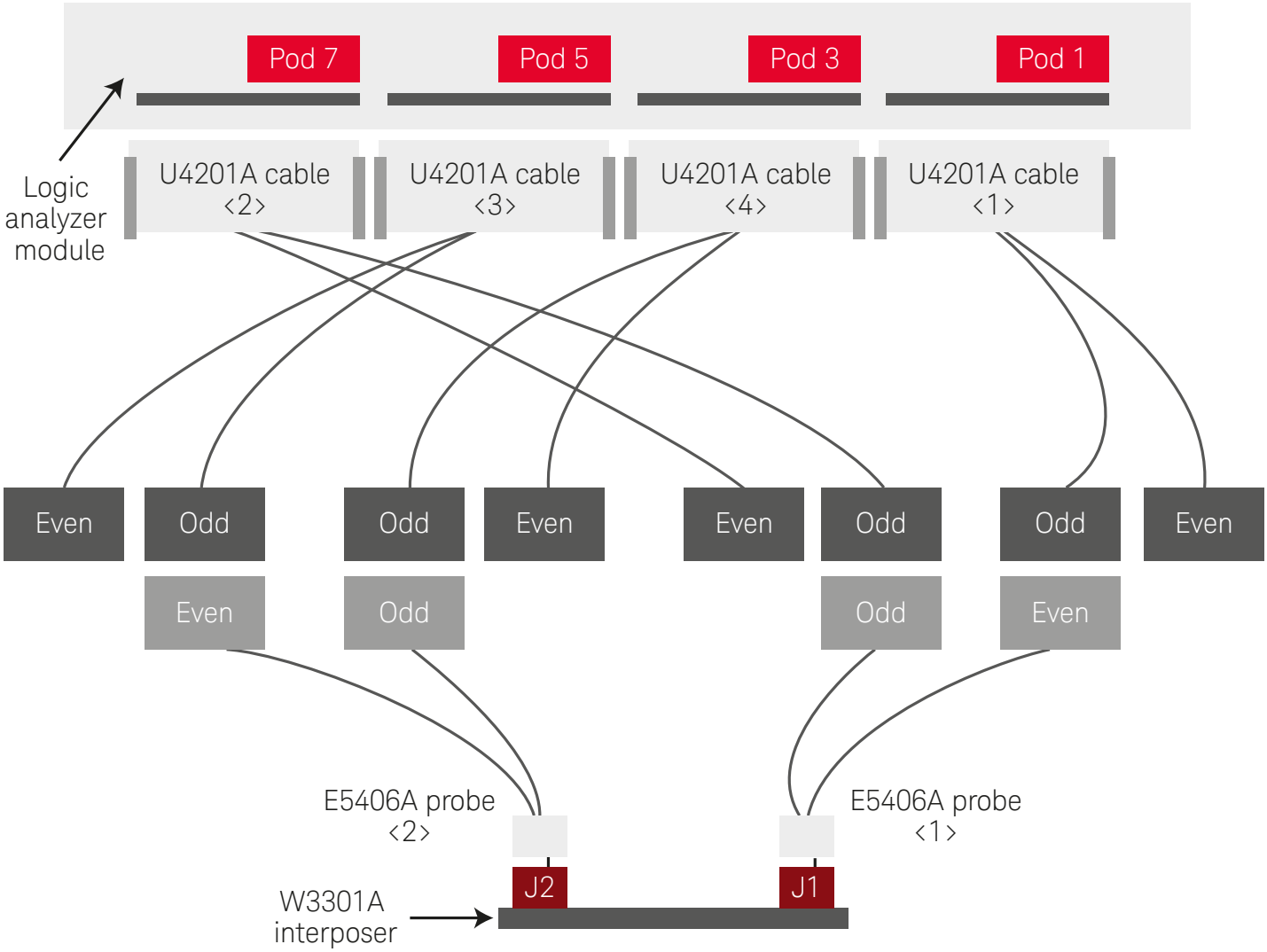


Figure 7. Connections between E5406A Soft Touch Pro probes and U4201A cables and logic analyzer pods.

Software

Default configuration for the W3301A interposer are included in the standard B4661A memory analysis software package. The Keysight B4661A memory analysis software provides four standard software features and four licensed memory analysis options.

B4661A standard software features

- Default configurations for DDR and LPDDR probing solutions for Keysight logic analyzers
- DDR setup assistant
- DDR eye finder/eye scan
- DDR configuration creator

The Keysight B4661A memory analysis software offers a suite of viewers and tools that include the industry's first protocol compliance violation testing capability across speed changes; a condensed traffic overview for rapid navigation to areas of interest in the logic analyzer trace; powerful performance analysis graphics; and DDR and LPDDR decoders. With the B4661A memory analysis software and a Keysight logic analyzer1, users can monitor DDR3/4 or LPDDR2/3/4 systems to debug, improve performance and validate protocol compliance. Powerful traffic overviews, multiple viewing choices, and real-time compliance violation triggering help identify elusive DDR/LPDDR system violations.

B4661A licensed software options

- DDR decoder with physical address trigger tool (Option-1NP/-1TP/-1FP)
- LPDDR decoder with physical address trigger tool for LPDDR/2/3 (Option-2NP/-2TP/-2FP)
- DDR and LPDDR compliance violation analysis toolset (Option-3NP/-3TP/-3FP)
- Post-process compliance violation analysis (Option-3NP/-3TP/-3FP)
- Real-time compliance violation analysis (Option-3NP/-3TP/-3FP)
- DDR3/4 and LPDDR2/3/4 performance analysis and ONFi analysis (Option-4NP/-4TP/-4FP)

DDR eye finder and eye scan software

DDR eye scan results of LPDDR3 signals gives you qualitative insight for all signals relative to each other. LPDDR3 signals are scanned in groups (Clock, CS#, ADD&Command, READ DQ/DQS, and WRITE DQ/DQS).

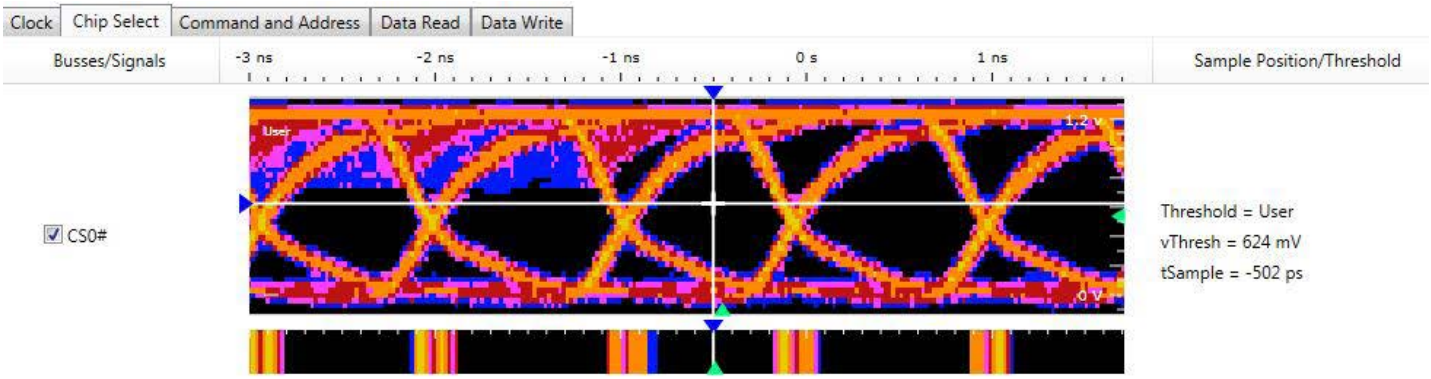


Figure 8. Eyescan of CS# shows large, clean eyes.

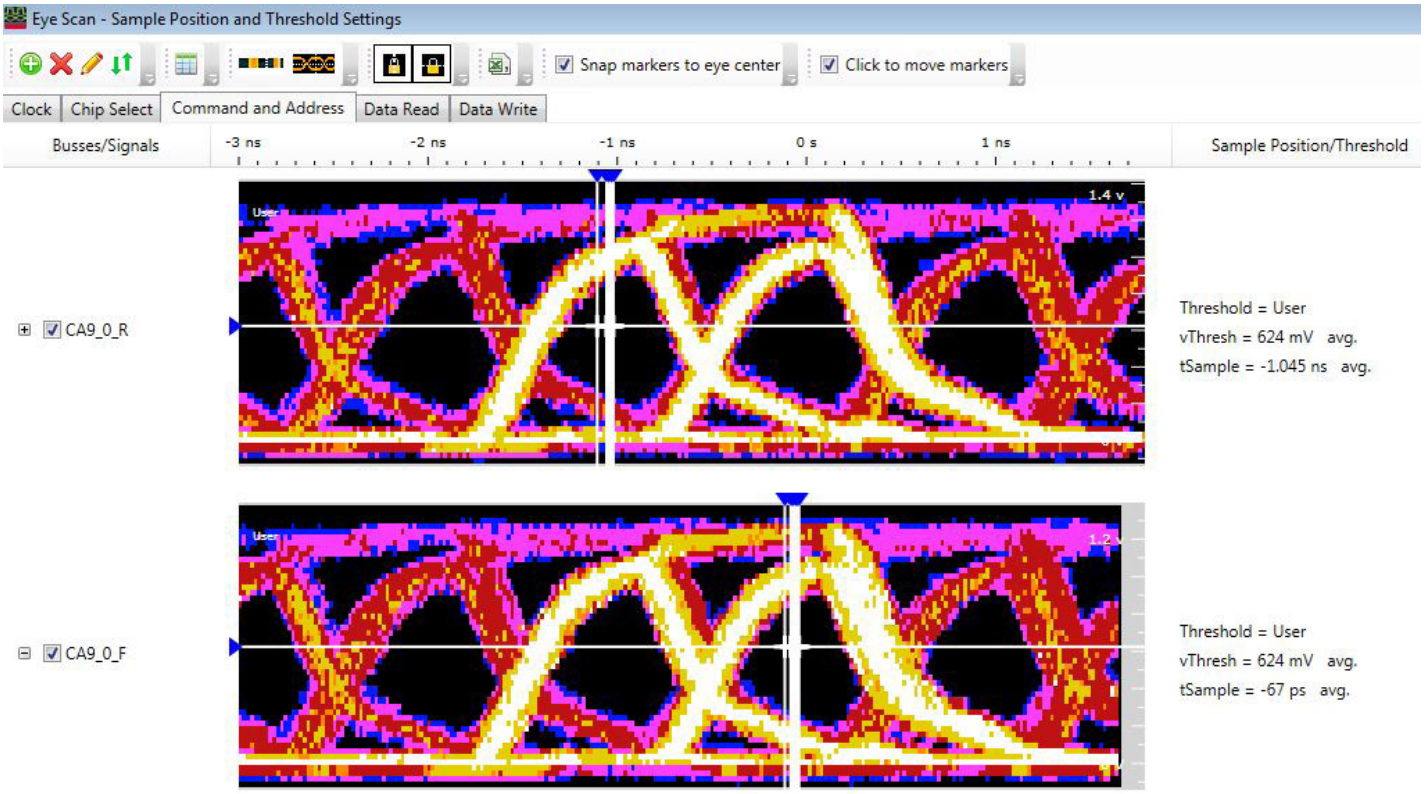


Figure 9. CA eye scans also show large, open eyes.

Note: The W3301A configuration has both CA9_0_R and CA9_0_F labels so that the users can set rising and falling edge sample positions. By capturing both the rising and falling edges simultaneously, the Keysight logic analyzer can easily trigger or search on specific physical addresses that occur on sequential CA edges on the LPDDR3 bus.

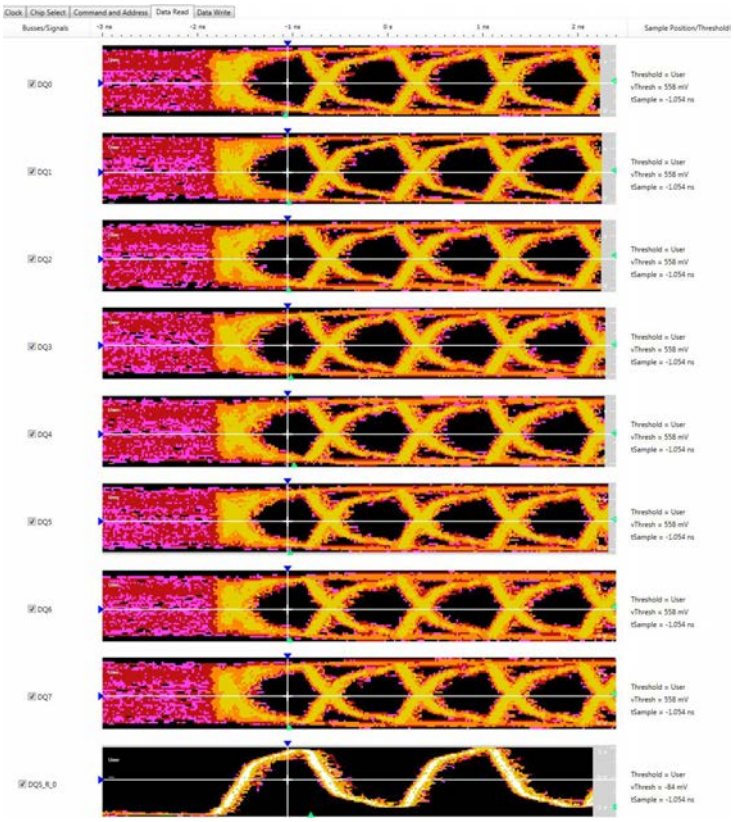


Figure 10. Read eye scans.

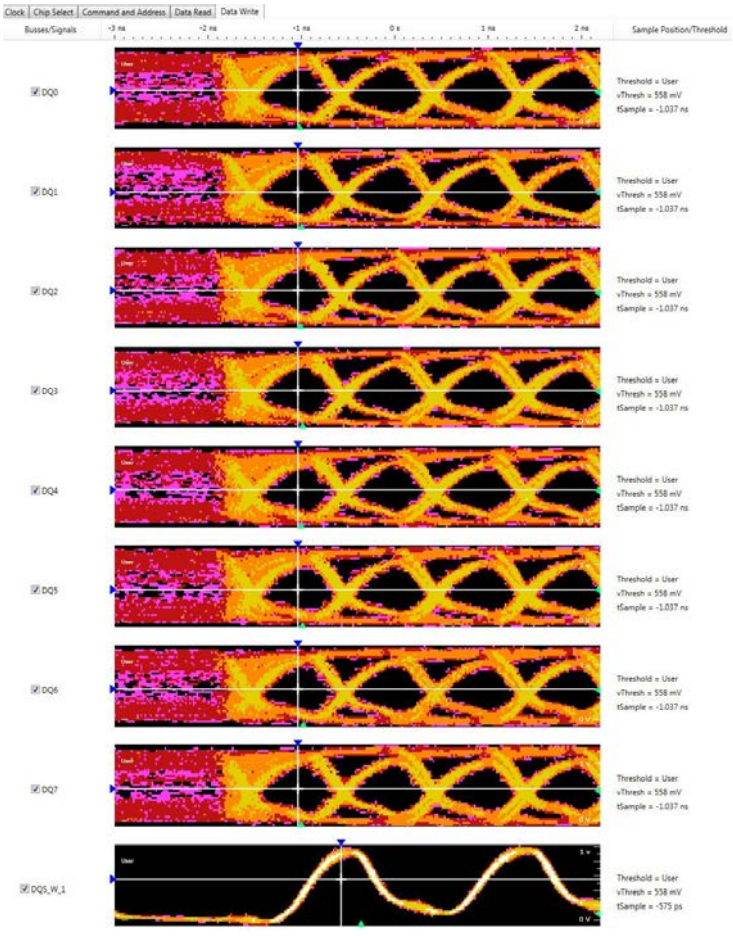


Figure 11. The LPDDR3 write eyes.

DDR and LPDDR performance analysis (B4661A-4FP/-4TP/-4NP)

Accelerate LPDDR3 analysis and debug using the B4661A memory analysis software licensed options.

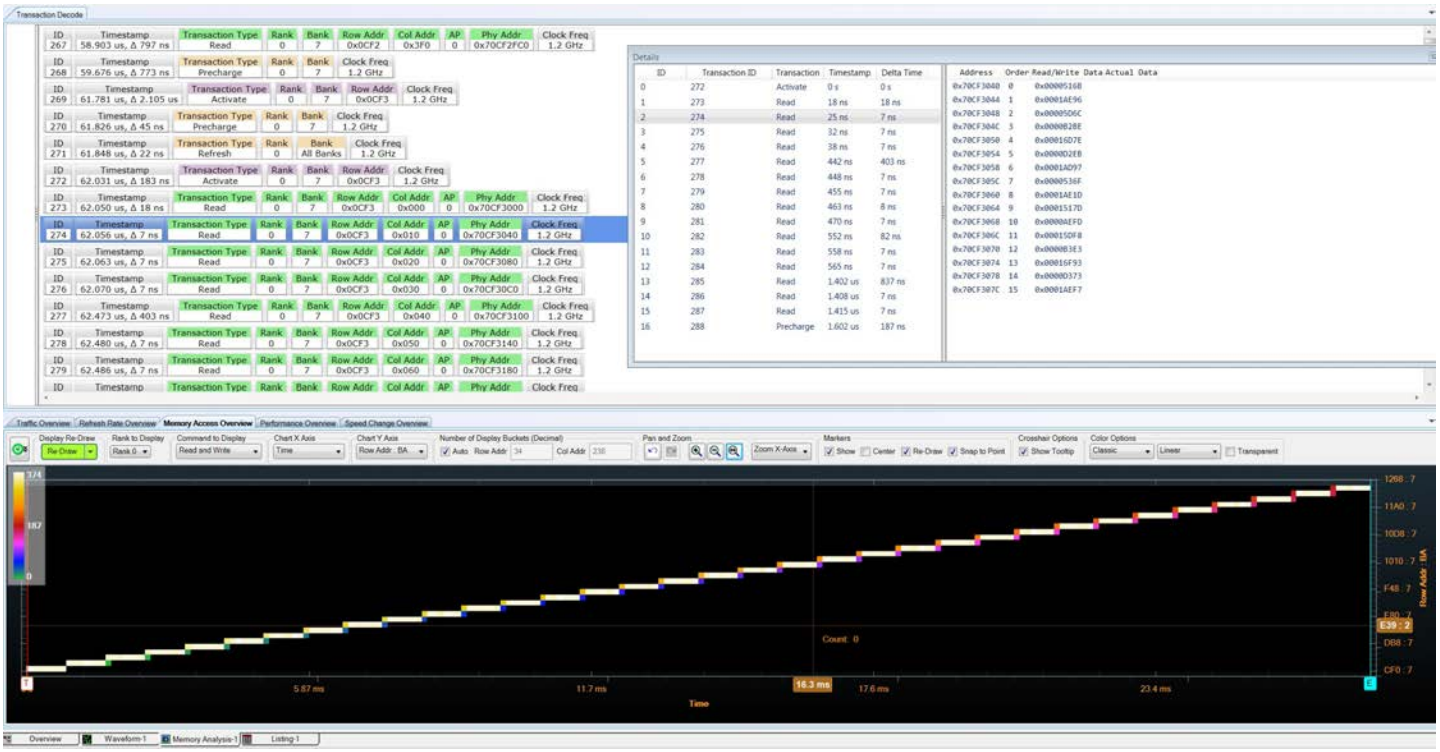


Figure 12. B4661A Option-4FP/-4NP/-4TP transaction decode, memory access overview graph and details window. (Image shown is LPDDR4 example.)

The memory analysis window, accessible from the overview window, is the B4661A-4FP/-4NP/-4TP option (performance analysis). All tabs in the memory analysis window are dockable and can be moved around for user viewing preference.

Benefits of the B4661A performance analysis transaction decoder and traffic overview

- Condensed view of all command activity in the trace
  - Including details of rank/bank, row, Col, BA, physical ADD, and clock frequency
- Enables rapid navigation of the trace
  - Click, scroll or jump to commands of interest
  - Pan/zoom on chart of command activity
  - Place or jump to markers (markers are global across all windows/views)
- Users can rapidly notice variations in charts of the command activity

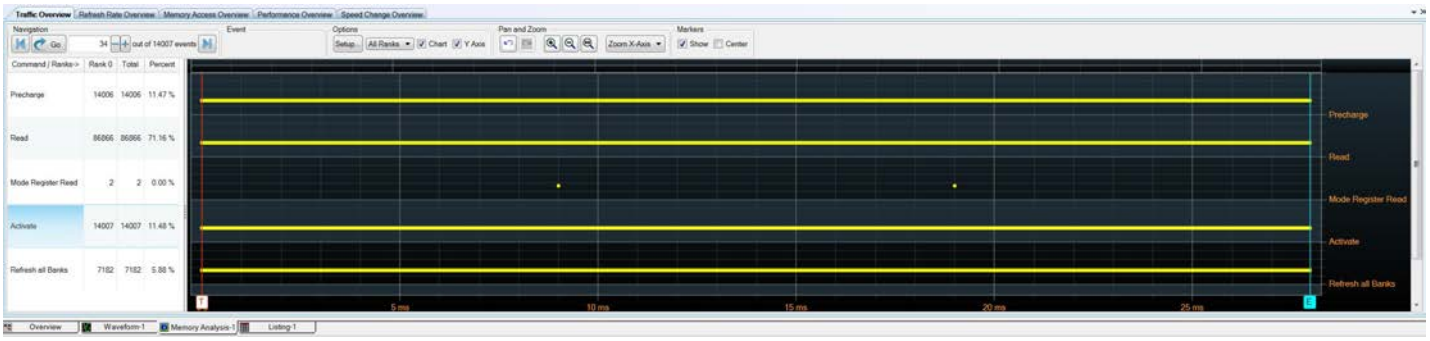


Figure 13. Traffic overview with graph is provided in the B4661A-4FP/-4NP/-4TP option. Notice that when you zoom in on the traffic overview graph you can see individual commands. In this trace, when all Ranks is selected, you only see one color (yellow) for Rank 0 as it is a single rank trace capture.

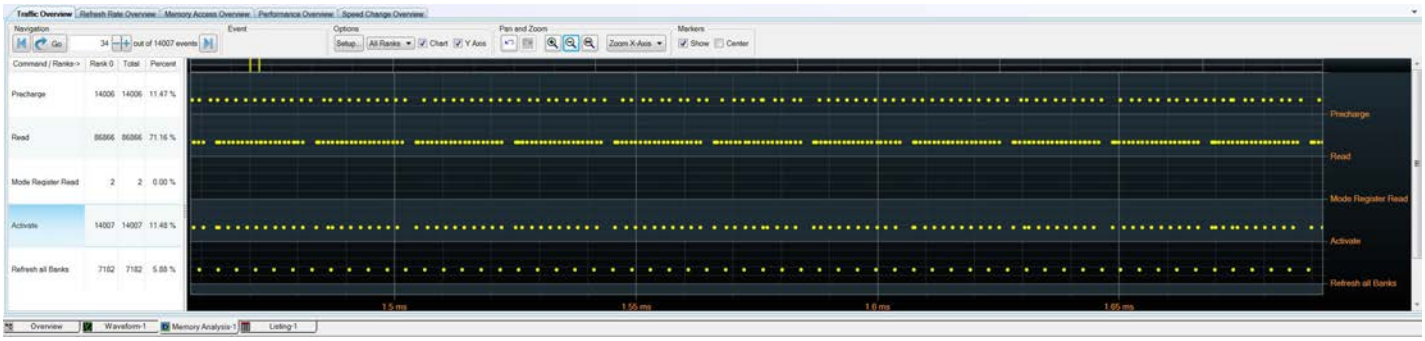


Figure 14. Zoom into details of command activity using traffic overview graph.

Details

ID	Transaction ID	Transaction	Timestamp	Delta Time
0	272	Activate	0 s	0 s
1	273	Read	18 ns	18 ns
2	274	Read	25 ns	7 ns
3	275	Read	32 ns	7 ns
4	276	Read	38 ns	7 ns
5	277	Read	442 ns	403 ns
6	278	Read	448 ns	7 ns
7	279	Read	455 ns	7 ns
8	280	Read	463 ns	8 ns
9	281	Read	470 ns	7 ns
10	282	Read	552 ns	82 ns
11	283	Read	558 ns	7 ns
12	284	Read	565 ns	7 ns
13	285	Read	1.402 us	837 ns
14	286	Read	1.408 us	7 ns
15	287	Read	1.415 us	7 ns
16	288	Precharge	1.602 us	187 ns

Address	Order	Read/Write Data	Actual Data
0x70CF3040	0	0x0000516B	
0x70CF3044	1	0x0001AE96	
0x70CF3048	2	0x00005D6C	
0x70CF304C	3	0x0000B2BE	
0x70CF3050	4	0x00016D7E	
0x70CF3054	5	0x0000D2EB	
0x70CF3058	6	0x0001AD97	
0x70CF305C	7	0x0000536F	
0x70CF3060	8	0x0001AE1D	
0x70CF3064	9	0x0001517D	
0x70CF3068	10	0x0000AEFD	
0x70CF306C	11	0x00015DF8	
0x70CF3070	12	0x0000B3E3	
0x70CF3074	13	0x00016F93	
0x70CF3078	14	0x0000D373	
0x70CF307C	15	0x0001AEF7	

Figure 15. Details tab available using B4661A-4FP/-4NP/-4TP performance analysis option.

The details tab provides additional information on commands.

DDR/LPDDR DRAM banks must be activated (opening a “page” or “row”) prior to any read/write activity to that bank/row. When the memory controller needs to access a different row address on the bank, a precharge is issued to “close” the “page.”

The all associated activates, reads, writes and precharges are displayed together on the left side of the details tab. This is important information for debug and performance optimization of a system. (Page violations can result in corrupt data and extra opening and closing of pages, which take time and slow system performance.)

On the left side of the details tab, you will see the data associated with any read or write command selected.

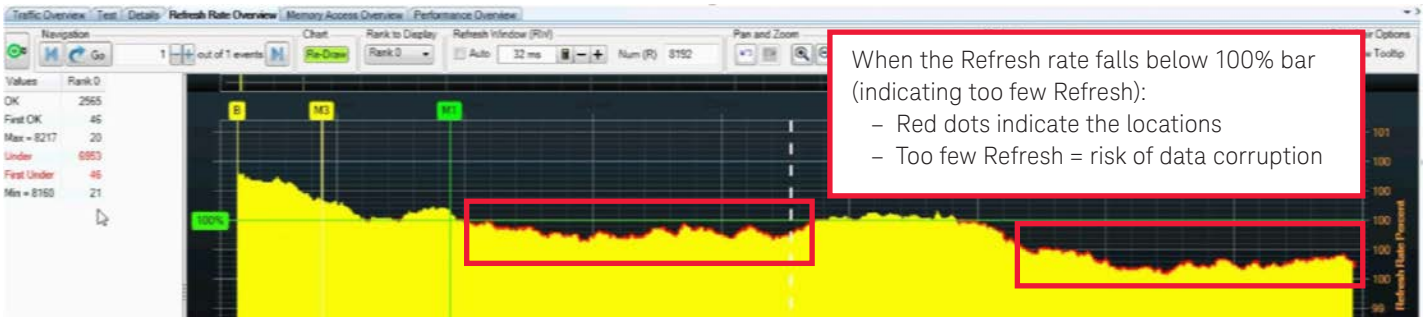


Figure 16. Refresh rate window. Included in the B4661A-4NP/-4TP/-4TP performance analysis option.

The refresh rate overview is an industry first. Analyzing a rolling 32 ms (adjustable) window of refresh activity to provide a percentage result for the minimum number of refreshes required (also adjustable). This new analysis view is particularly suited to viewing LPDDR refresh windows. Deep traces, usually 128 M or deeper are recommended for meaningful refresh rate displays.

The memory access overview in the B4661A-4NP/-4TP/-4FP option allows the user to select different X & Y variables to view the entire memory space accessed in the trace and to pan and zoom around the address space.

Time on the X and either BA:ROW or Row:BA are particularly insightful for highlighting “hot spots” of excessive activates to a particular blank/row address at a specific time. This can help users determine if particular memory tests or stimulus are possibly stressing row hammer. (Row hammer is a situation where internal rows on any specific bank inside the DRAM are victims of cross talk from surrounding rows in the bank.)

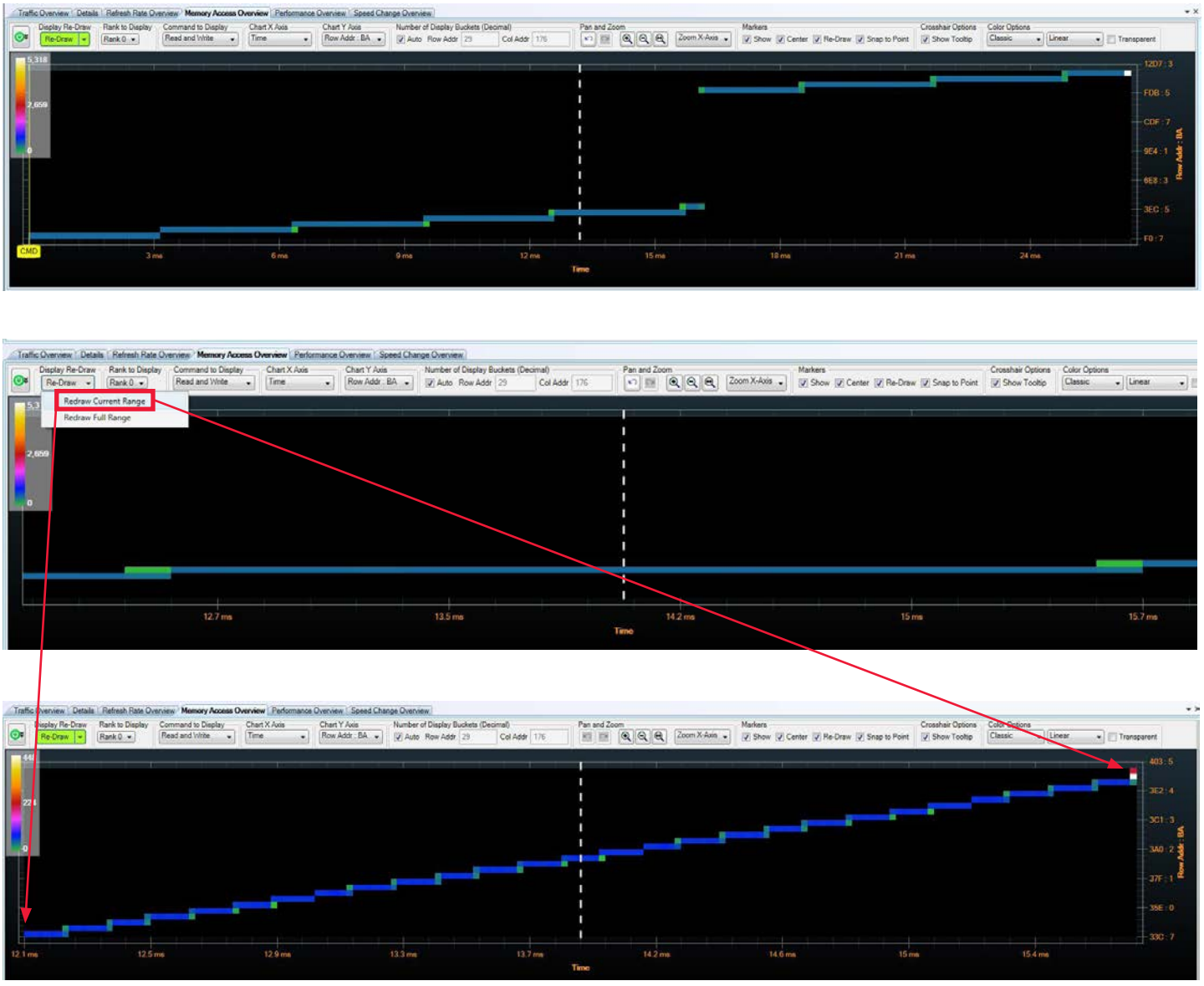


Figure 17. In memory access overview set for time vs. RowAdd:BA, the system under test was stepping through row addresses to individual banks. In this view, users can zoom in and re-draw to see more detail for a specific time.

Figure 18. Performance analysis overview. B4661A Option-4FP/-4NP/-4TP provides data rate performance and percent utilization analysis and graphs.

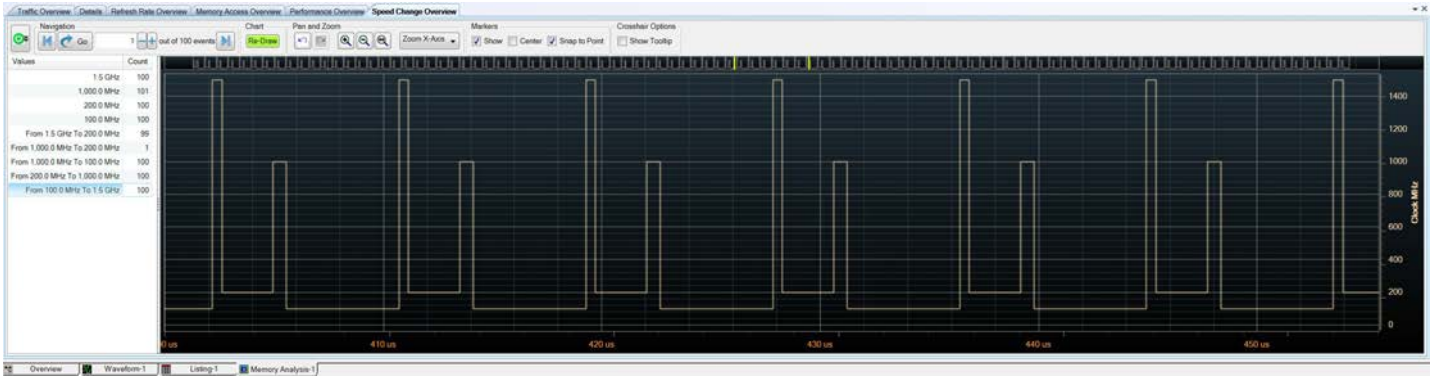


Figure 19. Clock frequency overview is provided in B4661A Option-4FP/-4NP/-4TP.

Clock frequency overview is very interesting to users with systems that are changing frequency. LPDDR systems can be aggressive at changing clock frequencies to conserve power.

DDR and LPDDR compliance violation analysis tool (B4661A-3FP/-3NP/-3TP)

The DDR and LPDDR compliance violation analysis toolset provides two tools under one license: post-process and real-time compliance violation. Both compliance tools cover DDR, DDR2, DDR3, DDR4, LPDDR, LPDDR2, LPDDR3 and LPDDR4.

Key features of both the post-process and real-time compliance violation tools:

- Test compliance violations across speed changes using the post-process compliance violation tool
- Identify DDR/2/3/4 or LPDDR/2/3/4 state machine, protocol compliance and protocol level bus cycle timing violations using either post-process or real-time tools
- Save time with automated real-time DDR2/3/4 or LPDDR2/3/4 protocol compliance measurements and trace captures using the real-time compliance violation analysis tool
- Edit parameters of the DDR/LPDDR standard preset tests easily using the enhanced parameter editing interface for both post-process and real-time tools

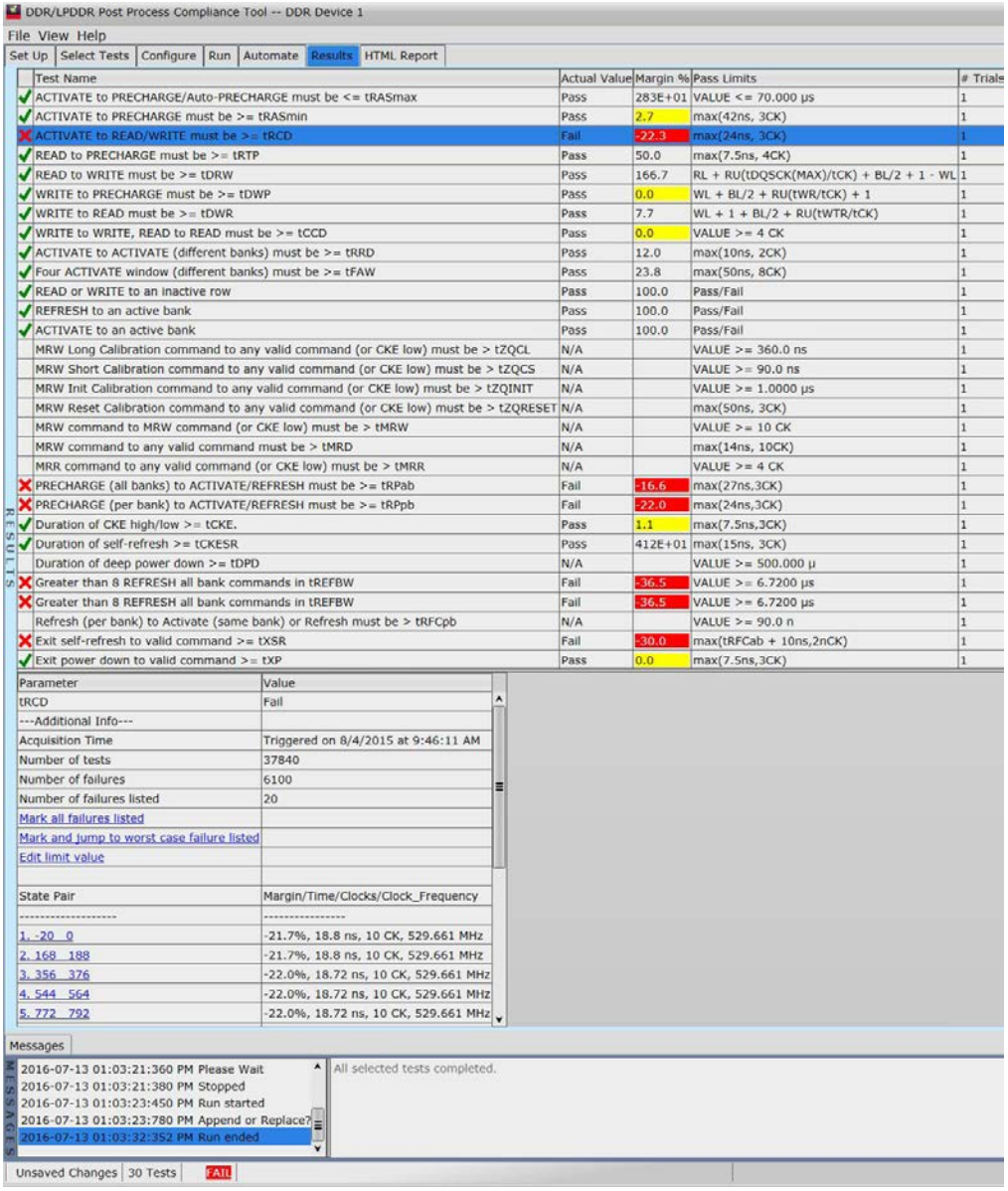
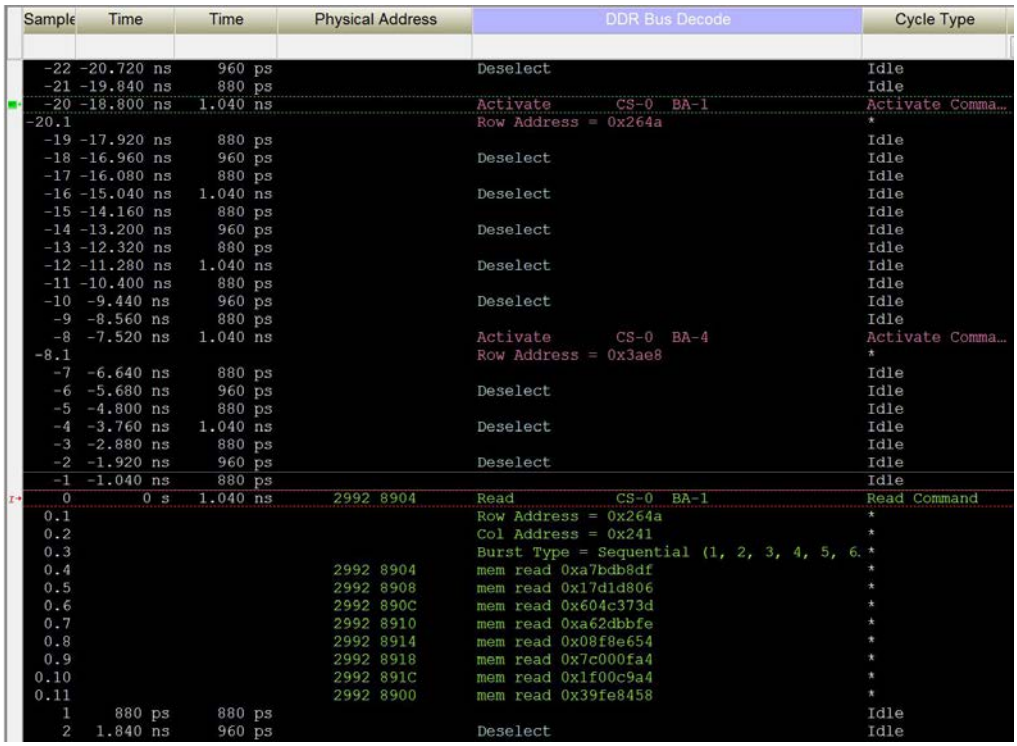


Figure 20. LPDDR3 post process compliance tests from B4661A Option-3FP/-3NP/-3TP.

LPDDR decode (B4661A-2FP/-2TP/-2NP)



Sample	Time	Time	Physical Address	DDR Bus Decode	Cycle Type
-22	-20.720 ns	960 ps		Deselect	Idle
-21	-19.840 ns	880 ps			Idle
-20	-18.800 ns	1.040 ns		Activate CS-0 BA-1	Activate Comma…
-20.1				Row Address = 0x264a	*
-19	-17.920 ns	880 ps			Idle
-18	-16.960 ns	960 ps		Deselect	Idle
-17	-16.080 ns	880 ps			Idle
-16	-15.040 ns	1.040 ns		Deselect	Idle
-15	-14.160 ns	880 ps			Idle
-14	-13.200 ns	960 ps		Deselect	Idle
-13	-12.320 ns	880 ps			Idle
-12	-11.280 ns	1.040 ns		Deselect	Idle
-11	-10.400 ns	880 ps			Idle
-10	-9.440 ns	960 ps		Deselect	Idle
-9	-8.560 ns	880 ps			Idle
-8	-7.520 ns	1.040 ns		Activate CS-0 BA-4	Activate Comma…
-8.1				Row Address = 0x3ae8	*
-7	-6.640 ns	880 ps			Idle
-6	-5.680 ns	960 ps		Deselect	Idle
-5	-4.800 ns	880 ps			Idle
-4	-3.760 ns	1.040 ns		Deselect	Idle
-3	-2.880 ns	880 ps			Idle
-2	-1.920 ns	960 ps		Deselect	Idle
-1	-1.040 ns	880 ps			Idle
0	0 s	1.040 ns	2992 8904	Read CS-0 BA-1	Read Command
0.1				Row Address = 0x264a	*
0.2				Col Address = 0x241	*
0.3				Burst Type = Sequential (1, 2, 3, 4, 5, 6…	*
0.4			2992 8904	mem read 0xa7bdb8df	*
0.5			2992 8908	mem read 0x17d1d806	*
0.6			2992 890C	mem read 0x604c373d	*
0.7			2992 8910	mem read 0xa62dbbfe	*
0.8			2992 8914	mem read 0x08f8e654	*
0.9			2992 8918	mem read 0x7c000fa4	*
0.10			2992 891C	mem read 0x1f00c9a4	*
0.11			2992 8900	mem read 0x39fe8458	*
1	880 ps	880 ps			Idle
2	1.840 ns	960 ps		Deselect	Idle

Figure 21. B4661A Option-2FP/-2NP/-2TP, LPDDR3 decode, viewed in listing window.

The B4661A-2FP/-2NP/-2TP offers a traditional LPDDR decoder for the logic analyzer listing window.

Benefits include:

- Complete decode of LPDDR commands with data associated to specific reads and writes
- Fastest display of decode (page aware)
- Users can scroll through the listing (or waveform) while computing large traces with the performance software

Configuration Guide and Ordering Information

W3301A includes

- LPDDR3 178-ball rigid BGA interposer
- 178-ball riser for devices under test that have components surrounding the LPDDR3 178-ball DRAM where the surrounding components are too close to install the W3301A without the riser. Riser includes a ground plane. Riser orientation is critical for proper operation.

W3301A requires

- Qty (2) E5406A Soft Touch Pro probes (each probe ships with a kit of 5 retention modules)
- Qty (4) U4201A cables to connect between the E5406A and compatible logic analyzer [1]
- Qty (1) U4164A logic analyzer module [2, 3, 4] in a chassis with a host controller

Optional for W3301A

- 178-ball riser for devices under test that have components surrounding the LPDDR3 178-ball DRAM where the surrounding components are too close to install the W3301A without the riser. Riser includes a ground plane. Riser orientation is critical for proper operation. Riser is included with the W3301A.
- The 178-ball riser may be replaced with an optional 178-ball grypper socket (sold separately): **http://www.hsiotech.com/products/released-products/engineering-products/grypper-family**.

Notes:

1. Qty (4) N2815A MSO/logic analyzer cable for connection to 90-pin logic analyzer probe can replace the U4201A cables. N2815A cables connect a single header into the odd pod of a U4164A pod pair. Therefore, they can't be used for applications where the even pod is required.
2. For data rates up to 1400 MT/s, the W3301A is compatible with the 16864A logic analyzer with Option 700.
3. The W3301A is also compatible with discontinued U4154A/B modules with appropriate speed grade options.
4. Minimum data valid window at the LPDDR3 DRAM balls requirements vary by logic analyzer module. U4164A has a small requirement at 100 mV x 100 ps. Termination settings and signal integrity of system under test affect data valid windows.

Recommended configuration

Item	Quantity
W3301A LPDDR3 178-ball BGA interposer	1
E5406A Soft Touch Pro probes	2
U4201A cables to connect between the E5406A probes and compatible logic analyzer	4
U4164A logic analyzer module	1
M9502A 2-slot chassis	1
M9537A embedded controller	1
B4661A-2FP/-2NP/-2TP LPDDR decoder	1
B4661A-3FP/-3NP/-3TP compliance analysis	1
B4661A-4FP/-4NP/-4TP performance analysis	1

Related Products

Product	Description
Modular logic analyzers	
U4164A	136-channel, up to 4 Gb/s state, quad state mode, up to 10 GHz timing, memory depth up to 400 M, AXIe-based logic analyzer module allowing three modules to merge into one time base
Logic analyzer probes/cables	
E5406A	Pro Series Soft Touch connectorless probe - single-ended, for 90-pin cable
U4201A	Logic analyzer cable
Software	
Logic and protocol analyzer software	Required – not licensed; acts as the base software platform
B4661A memory analysis	Required – unlicensed base software
	Licensed options recommended: Options-2FP/-2NP/-2TP, -3FP/-3NP/-3TP, -4FP/-4NP/-4TP
Portable logic analyzers	
16864A	136-channel, up to 1400 Mb/s state, dual sample mode, up to 10 GHz timing, memory depth up to 128

Related Literature

Publication title	Publication number
W3301A LPDDR3 DRAM BGA Interposer - Installation Guide	W3301-97000
Capture Highest DDR3 Data Rates Using Advanced Probe Settings on Logic Analyzers - Technical Brief	5991-0799EN
B4661A Memory Analysis Software for Logic Analyzers - Data Sheet	5992-0984EN
U4164A Logic Analyzer Module - Data Sheet	5992-1057EN
Probing Solutions for Logic Analyzers - Data Sheet	5968-4632E
Infiniium 90000 X-Series Oscilloscopes - Data Sheet	5990-5271EN

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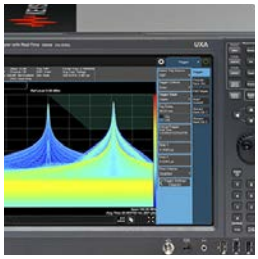

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Published in USA, November 29, 2016
5992-1682EN
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